AMENDMENTS TO THE SPECIFICATION:

Title:

Please amend the title as follows:

SEMICONDUCTOR PACKAGING DEVICE ~~AND MANUFACTURE THEREOF~~

On page 1 before BACKGROUND OF THE INVENTION, *please insert the following paragraph:*

This application is a continuation application of U.S. Application No. 10/074,052.

Please amend the paragraph beginning on page 1, at line 9 as follows:

The invention relates to a stacking semiconductor packaging device and manufacture thereof, and more particularly relates to a ~~structure of flip chip ball grid array (FCBGA) and manufacture thereof~~ semiconductor packing device with a carrier for chip.

Please amend the paragraph beginning on page 2, at line 15 as follows:

It is another object of the present invention to provide improved structure of FCBGA and manufacture thereof. The redistribution and solder-bump process for a conventional structure of FCBGA are simplified and integrated into the fan-out process of build-up substrate.

Please delete the paragraph on page 2, beginning at line 26 in its entirety and replace it with the following new paragraph:

A semiconductor packaging device provides a carrier having at least a portion configured for containing a chip. The chip, affixing to the portion with sidewall, has a back surface an active surface, which multitudes of bonding pads are on the active surface. One insulating layer on the active surface and carrier has multitudes of conductive holes corresponding to the first bonding pads. A multi-layer structure on the insulating layer is configured for providing electrical connection to the conductive holes. Another insulating layer, affixed on one of the carrier and the multi-layer structure, has another conductive holes electrically connected to the

conductive holes. Multitudes of solder balls, on at least one of the carrier and latter insulating layer, electrically connect the latter conductive holes. Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.

Please delete the paragraph beginning on page 5, beginning at line 8 in its entirety and replace it with the following new paragraph.

A semiconductor packaging device provides a carrier having at least a portion configured for containing a chip. The chip, affixing to the portion with sidewall, has a back surface an active surface, which multitudes of bonding pads are on the active surface. One insulating layer on the active surface and carrier has multitudes of conductive holes corresponding to the first bonding pads. A multi-layer structure on the insulating layer is configured for providing electrical connection to the conductive holes. Another insulating layer, affixed on one of the carrier and the multi-layer structure, has another conductive holes electrically connected to the conductive holes. Multitudes of solder balls, on at least one of the carrier and latter insulating layer, electrically connect the latter conductive holes.

Please amend the paragraph beginning on page 7, at line 22 as follows:

FIGS. 3-5 are cross-sectional views illustrating the packaging chip cut with line 2A-2A of FIG. 2. Depicted in FIG. 3, solder balls are distributed on the surrounding of the chip. After the chip 20 is placed in the carrier 11 and affixed by an adhesive 19, an insulating layer 14 is formed on the active surface 30 of the chip 20 and the carrier 11 where the bonding pads 21 of the chip 20 are exposed. Multitudes of plating through hole 22 in the insulating layer 14 are corresponding and electrically connected to the bonding pads 21. A multi-layer film 15 with predetermined circuit 23 and plating through holes 22 is on the insulating layer 14 and thereafter another insulating layer 16 is formed on the multi-layer film 15 only to expose the pads 18 of the plating through holes 22 on which the solder balls 17 are affixed, and the solder balls are distributed on the carrier 11, the chip 20, or both. Thus, the pad redistribution, bumping, and fan-out processes for the chips can be implemented at ~~one time~~ same process. One of advantages of the present invention is to avoid the direct chip attachment to a print circuit board for fear of